Remarks

Claims 1-14 are pending in the application. It is noticed again that the Office Action Summary still mentions about claims 1-13 only, whereas the Detailed Action duly addresses all claims 1 through 14. It is therefore considered that mention of claims 1-13 instead of claims 1-14 in the Office Action Summary is due to a repetition of the typographical error which had already been indicated in the response to the previous Office Action.

Claims 1-5 and 7-14 are rejected.

Claim 6 is objected to.

Allowable Claims

The Examiner is thanked for the indication that Claim 6 would be allowable if rewritten in independent form. However, because the Applicant believes that the remaining claims in this application are also allowable, the Applicant has not rewritten Claim 6 in independent form.

Rejection under 35 U.S.C. § 103

It is hereby acknowledged that the rejection under 35 U.S.C. § 102(e) based on U.S Patent Publication No. 6,693,494 to Fan *("Fan")*, which was contained in the previous Office Action, dated September 26, 2007, is not maintained in the present Office Action.

Indeed, the Examiner correctly indicates that *Fan* fails to disclose at least one series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator, as was extensively discussed in the paper filed in response to the previous Office Action.

The present Office Action, however, rejects Claims 1, 7 and 10-14 under 35 U.S.C. § 103, as being unpatentable over *Fan* in view of *Nilson and Riedel*, "Electric Circuits", Fifth Edition, Figure 6.17, page 227. The Applicants respectfully traverse this rejection.

Fan discloses a phase locked loop (PLL) that includes a phase comparator (PFD), a charge pump, a loop filter and a voltage controlled oscillator (VCO) in the main path, and a fractional-N frequency divider in the return path. In his analysis of *Fan* for the assessment of the inventive step of the claimed subject-matter, the Examiner equates the claimed voltage shift capacitor with capacitor C1 or, more probably with capacitor C3 shown in Figure 6 of *Fan*. However, neither C1 nor C3 is a series capacitor coupling the phase comparator and the VCO.

It seems necessary to first recall what, in the field of electronic circuit design, is meant by a series capacitor, as opposed to a parallel capacitor.

As is well known by the one with ordinary skills in the art, a "series capacitor" is a capacitor which is connected between (the output node of) a circuit A, and (the input node of) a circuit B within a given design. Such connection in series of a capacitor C is illustrated by FIG. 1 herein below:

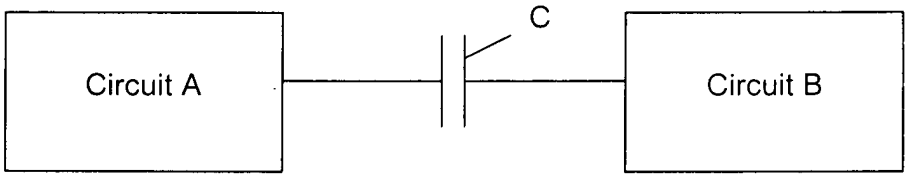

FIG.1: Capacitor C connected in series between Circuit A and Circuit B

On the contrary, a "parallel capacitor" is known as a capacitor which is connected between a given node D of a design, let us say the node which corresponds to the output of a circuit A and/or the input of a circuit B, on the one side, and the ground, on the other side. Such parallel connection of a capacitor C is illustrated by FIG. 1 herein below:

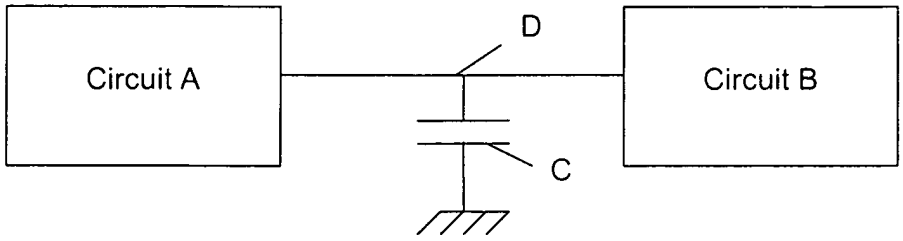

FIG. 2: Capacitor C connected in parallel between Circuit A and Circuit B

In the independent claims of the present application, there is recited "at least one series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase locked loop", which corresponds to the case illustrated by above FIG. 1. The Examiner is invited to further refer to Figures 2 and 6 of the application, which show the connection of capacitor Ca between nodes 21 and 22, which are the output of the PFD and the input of the VCO, respectively.

Figure 6.17 of *Nilson and Riedel*, which is relied upon by the Examiner, relates to connection of a plurality of capacitors C1, C2, ... Cn in series one with the others, which provides equivalent capacitance value as a single capacitor Ceq, whose value satisfies the equation (6.28). Actually, *Nilson and Riedel*, discloses the well known rule that the a combination of a plurality of capacitors connected in series is equivalent to a single capacitor, the admittance 1/Ceq of which is equal to the sum 1/C1 + 1/C2 + ... + 1/Cn of the admittances of the plurality.

For the purpose of responding to the rejection of the independent claims it is assumed that the Examiner considers that *Nilson and Riedel*, motivates the one with ordinary skills in the art to replace one single capacitor by a plurality of capacitors connected in series one with the others. Nevertheless, *Nilson and Riedel* is silent about whether the single equivalent capacitor and/or the plurality of capacitors connected in series, operate as a series capacitor or as a parallel capacitor in the meaning which has been recalled above in view of FIG. 1 and FIG. 2. This is because *Nilson and Riedel* relates to a capacitor out of its context of use.

Stated otherwise, *Nilson and Riedel*, does not relate to the relationship between a series capacitor as depicted in FIG. 1 and a parallel capacitor as show in FIG. 2. Actually, there exists no specific such relationship, the respective operational behavior of a series capacitor and of a parallel capacitor of same value being dependent on extrinsic considerations only, such as the frequency of the signals going through said capacitors. For instance, a series capacitor usually acts as high pass element which lets signals above a certain frequency go through and blocks signals under that frequency. On the contrary, a parallel capacitor sinks signals above a certain frequency to ground, and therefore usually participates to a low pass configuration. Typically, a loop filter of a VCO usually comprises a parallel capacitor acting as a sink for signal components at high frequencies. See for instance capacitor C1 of loop filter 20 in Figure 2 of the application, and description page 5 lines 13-24.

To conclude, *Nilson and Riedel* fails to remove the deficiencies in *Fan*. Besides, the one with ordinary skills in the art, considering the disclosure in *Fan*, would not even see a reason to consult *Nilson and Riedel*, was he faced with the problem of adapting the circuit in *Fan* to a series capacitor.

In addition, and as was already put forward in the response to the previous Office Action, even if one could isolate the means 62, 63, 64, 65, Sb and Sc of the loop filter 22 of *Fan* from the rest of the elements which are present between the output of the PFD and the input of the VCO of *Fan* (and name them, according to the Examiner's analysis of *Fan*, a "voltage shift control circuit"), it would remain the following differences with the claimed invention:

- these means of *Fan* which the Examiner wrongly identifies with the controlled charging means and controlled pre-charging means of the invention are comprised in the loop filter 22 of *Fan*, which is not at all a circuit adapted for being placed in parallel with a series voltage shift capacitor, but rather a circuit connected in parallel between the node defined by the input of the VCO and the ground;
- these means 62, 63, 64, 65, Sb and Sc of *Fan* do not provide the feature of the claimed

controlled polarization means. The Examiner refers to the 1-bit quantizer 40 shown in Figure 4 of *Fan*, which is comprised in the low pass filter 29 of Figure 3 of *Fan*. However, there is absolutely no disclosure in *Fan* to support the Examiner's statement that *Fan* teaches that the 1-bit quantizer allows to ensure the polarization of the input of the voltage shift control circuit (identified with the output of the PFD by the Examiner). *Fan* only discloses (see paragraph [0032] of *Fan*) that the 1-bit quantizer allows to speed-up the discharging of the capacitor C of the low pass filter 29.

Therefore, even if *Fan* and *Nilson and Riedel*, were combined by the one with ordinary skills in the art in the manner and with the result stated by the Examiner, it would not arrive at the combination of features according to the independent claims.

For the above reasons, the Office Action has not shown that the combination of *Fan* and *Nilson and Riedel* anticipates the Applicant's invention as recited in Claims 1, 7 and 10-14. Accordingly, the Applicants respectfully request withdrawal of the § 103 rejection and full allowance of Claims 1, 7 and 10-14.

Rejection of the Dependent Claims

Claims 2-5, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,693,494 to *Fan* in view of U.S. Patent No. 6,611,161 to *Kumar et al* and further in view of *Nilson and Riedel.* This rejection is respectfully traversed.

Indeed, Claims 2-5, 8 and 9 are dependent claims that depend directly or indirectly on independent claims which are deemed allowable for the reasons set forth above.

Therefore, they are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

Conclusion

Given the above remarks, the independent claims are believed to be in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (312) 263-4700.

Reconsideration and allowance of the foregoing claims are respectfully requested.

Deposit Account Authorization

The Commissioner is hereby authorized to charge any deficiency in any amount enclosed or any additional fees which may be required during the pendency of this application under 37 CFR 1.16 or 1.17, except issue fees, to Deposit Account No. 50-1903.

Respectfully submitted,

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By: 

January 6, 2009

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